Wrexham glyndŵr UNIVERSITY

MODULE SPECIFICATION

Module Title:	**Electronics, Design and Testing**	**Level**:	6	**Credit Value**:	20

Module code:	ENG60D	**Is this a new module?** Yes	**Code of module being replaced**:	ENG60C

Cost Centre:	GAEE	**JACS3 code**:	H650

Trimester(s) in which to be offered:	1 & 2	**With effect from:**	September 18

School:	Faculty of Arts, Science and Technology	**Module Leader:**	Andrew Sharp

Scheduled learning and teaching hours	60 hrs
Guided independent study	140 hrs
Placement	0 hrs
Module duration (total hours)	200 hrs

Programme(s) in which to be offered	Core	Option
BEng (Hons) Electrical and Electronic Engineering	✓	☐

Pre-requisites
None

Office use only

Initial approval February 17

APSC approval of modifications, Sept 18, June 2020 Version 2

Have any derogations received Academic Board approval? Yes ✓ No ☐

Module Aims

1. To build upon analytical skills and knowledge gained in previous modules to further develop students' problem-solving abilities relating to the design, analysis and evaluation of electrical and electronic systems in a variety of applications;

2. To extend the student to develop original test strategies and to consider the interrelationships of test and design within the design and manufacturing cycle for modern electronic products.

Intended Learning Outcomes

Key skills for employability

KS1	Written, oral and media communication skills
KS2	Leadership, team working and networking skills
KS3	Opportunity, creativity and problem solving skills
KS4	Information technology skills and digital literacy
KS5	Information management skills
KS6	Research skills
KS7	Intercultural and sustainability skills
KS8	Career management skills
KS9	Learning to learn (managing personal and professional development, self-management)
KS10	Numeracy

At the end of this module, students will be able to		Key Skills
1	Originate designs for a given specification	KS6
2	Design and develop electronic circuits for instance: cascade circuits, cascode circuits, passive and active nth order filters.	KS3
3	Analyse test requirements during the design stages of an electrical or electronic circuit or system, and incorporate suitable improvements to enable flexible, cost effective automatic testing.	KS3
4	Analyse Hardware, specify, and design appropriate software algorithms and test equipment to implement accurate and cost effective tests by means of a minimal test programme; automatic testing for industrial product inspecting, quality control and improvement.	KS5
5	Use analysis techniques, including computer modelling techniques and practical experiments to verify and assess theoretical predictions and evaluate the performance of a given design.	KS4

Transferable/key skills and other attributes

1. Apply analysis techniques;
2. Solve problems;
3. Apply design.

Derogations

A derogation from regulations has been approved for this programme which means that whilst the pass mark is 40% overall, each element of assessment (where there is more than one assessment) requires a minimum mark of 30%.

Assessment:

Assessment One: is by means of a major practical assignment. For example: individual design and implementation of test sequences using automated hardware programmed using industry leading software. The equipment can be used to control dc/ac sources, DMM/DSO etc to automatically characterise a given item under test. e.g. Component / Analogue Amp / Digital logic PCB/PV panel etc. The evidence of the activity is produced as a portfolio of software, written report and a final practical demonstration of the solution. It covers outcomes 3, 4 and 5.

Assessment Two: is by means of an examination covering outcomes 1, 2, and 3. It is an unseen time-constrained examination with a fixed number of questions, typically five, where students are required to answer only three out of the five possible.

Assessment number	Learning Outcomes to be met	Type of assessment	Weighting (%)	Duration (if exam)	Word count (or equivalent if appropriate)
1	3,4,5	Portfolio	50		2000
2	1,2,3	Examination	50	2 hrs	

Learning and Teaching Strategies:

The module will be delivered mainly through lectures and student-driven development work, particularly using computer-based, automated test equipment. A significant amount of the work is carried out by students in a minimally supervised specialist lab accessed outside normal class times.

Detailed lecture notes provided for the student will allow the optimisation of lecture time, with good opportunity for self-study and ad hoc tutorials. Case studies may be used using examples of failure obtained from our commercial activities for industrial companies and are designed to broaden the range of students reading and may help with their practical work.

Extensive use will be made of VLE (Moodle) to supplement learning materials and provide on-line quizzes for additional learning opportunities.

Syllabus outline:

Design:

Operational amplifiers: Electrical characteristics of operational amplifiers; internal structure, differential amplifier, current mirrors, dynamic loads, level shifting and complementary class B output stages.

The ideal operational amplifier; summing, differentiating, logarithmic function; antilog, integrator and differentiator. Selection criteria for op-amps and practical limitations. Methods of eliminating output voltage offsets and suitable noise models.

Signal generation: Position fullwave and halfwave active rectifier circuits. Waveform generators and Schmitt trigger circuits.

Transistor/FET modelling at high and low frequencies (CE-CS, CB-CG, CC-CS).

The nature of filters; S plane transfer characteristics and models for low/high pass systems and high/low pass transformations.

Active filters: Sallen-key and multiple feedback**,** analysis of Butterworth/Bessel and Chebyshev with high/low and bandpass transformations.

Testing:

Testing methodology: The Design cycle, test strategies and use of manual, automatic and semi automatic test implementations for industrial product inspecting, quality control and improvement, analysis of design, manufacturing, random and end of life faults. Design of structured testing algorithms for circuits and systems, test pattern generation, minimal and fault location algorithms. Analogue/digital and power system techniques.

Designing for testability: Principles, integration of test considerations into the design cycle, reliability and maintainability considerations. Testability measures and good practices. Relevance to QA and QC. Costs and penalties. Feedback from manufacture, test and field failures, safety, costs, timescales, RoHS.

Parametric analysis: Derivation of design and test limits, use of tolerance tiering, statistical analysis of production data, trend analysis and monitoring techniques.

Advanced test features: Overview: Boundary Scan, BILBO, etc. Self-test features, and comparison of algorithmic-based techniques with knowledge-based systems; suitability for ATE.

Current developments and Applications: Investigation and review by, attendance at seminars, guest speakers (Researchers, KTP and placements, etc), review of manufacturers' web based literature and software, Case studies, Identification of parametric, functional and test anomalies during complex system integration, etc. Automatic electronic testing systems in process quality control and improvement.

Implementation: Design of ATE systems incorporating ergonomic considerations, safety, initialisation, fault handling.

Bibliography:

Essential reading

Crecraft, D.I and Gorham, D.A. (2003) *Electronics*, 2nd Edn., Nelson Thornes Ltd.

Other indicative reading

Angus, R.B. and Hulbert, T.E. (2005) *VEE Pro Practical Graphical Programming*, London: Springer.

Crouch, A. (1999) *Design for Test*, London: Prentice-Hall.

O'Connor, P.D.T (2001) *Test Engineering,* New York: John Wiley and Sons.

Various (2007-…) *Components in Electronics* http://www.cieonline.co.uk London Newsquest Specialist Media.

Various (2007-…) *Electronics Weekly* http://www.electronicsweekly.com London Reed Business Information 24.